We Claim:

1   1.   An integrated memory, comprising:

2   a plurality of memory cells in a memory cell array, the memory cells being

3   combined to form individually addressable normal units;

4   a plurality of redundant units of memory cells for respectively replacing one of

5   the normal units on an address basis;

6   a memory unit for storing, in a normal mode, an address for one of the normal

7   units which needs to be replaced by one of the redundant units;

8   a comparison unit, the comparison unit being connected to an address bus in the

9   memory and to an output of the memory unit for the purpose of comparing an address

10   which is present on the address bus with an address stored in the memory unit and for the

11   purpose of activating one of the redundant units in the event of a match being identified;

12   and

13   a test circuit, the test circuit being activated by a test mode signal, and the test

14   circuit adapted to reset the memory unit to an initial state and to store an address for one

15   of the redundant units in the memory unit for subsequently writing to the redundant unit.

1   2.   The integrated memory as claimed in claim 1, wherein the memory unit is

2   programmable, the memory has a second nonvolatile memory unit for permanently

3   storing an address, the memory further having and has at least one output which is

4   connected to a corresponding input of the memory unit for transmitting an address stored

5   in the second memory unit to the programmable memory unit.

1   3. The integrated memory as claimed in claim 2, wherein the second nonvolatile

2 memory unit can be programmed only once.

1   4. The integrated memory as claimed in claim 2, wherein the second nonvolatile

2 memory unit has laser fuses, which can be programmed from outside the memory by a

3 laser beam.

1   5. The integrated memory as claimed in claim 1, wherein the memory is in the

2 form of a DRAM.

1   6. The integrated memory as claimed in claim 1, wherein the memory unit is in

2 the form of a register having register elements for storing a respective address bit.

1   7. A method for testing an integrated memory, the integrated memory having a

2 plurality of memory cells in a memory cell array, the memory cells being combined to

3 form individually addressable normal units, a pluarlity of redundant units of memory

4 cells for respectively replacing one of the normal units on an address basis, a memory

5 unit for storing, in a normal mode, an address for one of the normal units which needs to

6 be replaced by one of the redundant units, a comparison unit which is connected to an

7 address bus in the memory and to an output of the memory unit for comparing an address

8 which is present on the address bus with an address stored in the memory unit and for

9 activating one of the redundant units in the event of a match being identified, the method

10 comprising:

11   activating a test mode;

12   resetting the memory unit to an initial state;

13   storing an address for one of the redundant units in the memory unit;

14   writing an identification code to the one of the redundant units;

15   deactivating the test mode;

16   setting the memory unit using the address for one of the normal units which needs

17 to be replaced;

18   accessing the memory cell array;

19   applying addresses for normal units to the address bus for reading the memory

20 cell array;

21   reading the memory cell array; and

22   associating the identification code which is read with the address for the normal

23 unit addressed for this reading operation.